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**Pick-up for CCD image sensor - produces signal having reference and
signal component derived from capacitor in response to output charge from
CCD element**

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Patent Family:

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DE 3106359	A	19820211	DE 3106359	A	19810220	198207
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Abstract (Basic): GB 2071959 A

The arrangement comprises a solid state image pick-up device including charge transfer elements - e.g. CCD's - for producing elemental output charges corresponding to an image. During each elemental output interval (Tan B), there is produced in sequence a reference level portion (TP) and a signal portion (TS) which is derived by charging or discharging a capacitance in response to the output charge.

Both the reference level portion and the signal portion may be contaminated with noise (N). The noise is therefore removed by deriving the difference between the reference level portion and the signal portion. The difference is produced by a differential amplifier (16), either fed with the signal both direct, and via a delay (15) and followed by a sample and hold circuit (10). Alternatively, sample and hold circuits may be used to provide sampling and for holding the reference level portion and signal portion for simultaneous comparison.

3+4

Title Terms: PICK-UP; CCD; IMAGE; SENSE; PRODUCE; SIGNAL; REFERENCE; SIGNAL ; COMPONENT; DERIVATIVE; CAPACITOR; RESPOND; OUTPUT; CHARGE; CCD; ELEMENT

Index Terms/Additional Words: CHARGE; COUPLE; DEVICE

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(54) Signal pick-up circuit arrangements

(57) In a signal pick-up circuit arrangement comprising a solid state image

pick-up device including charge transfer elements - eg CCD's - for producing elemental output charges corresponding to an image, wherein during each elemental output interval (τ_B), there is produced in sequence a reference level portion (T_P) and a signal portion (T_S) which is derived by charging or discharging a capacitance in response to the output charge, both the reference level portion and the signal portion may be contaminated with noise (N). The noise is therefore removed by deriving the difference between the reference level portion and the signal portion.

The difference is produced by a differential amplifier (16), either fed with the signal both direct, and via a delay (15) and followed by a sample and hold circuit (10), or by sample and hold circuits, sampling and holding the reference level portion and signal portion for simultaneous comparison.

FIG. 3

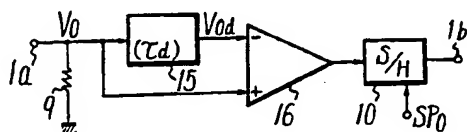
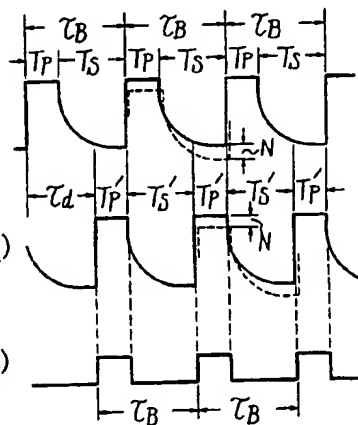


FIG. 4A (V_0)

FIG. 4B (V_{0d})

FIG. 4C (SP_0)



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FIG. 1

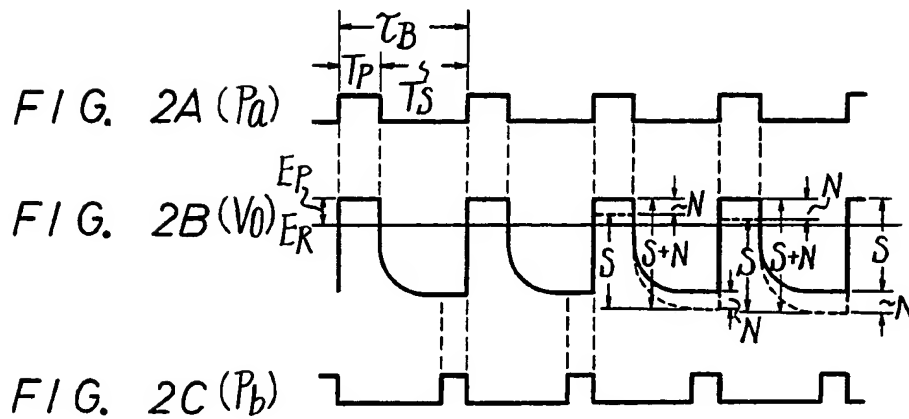
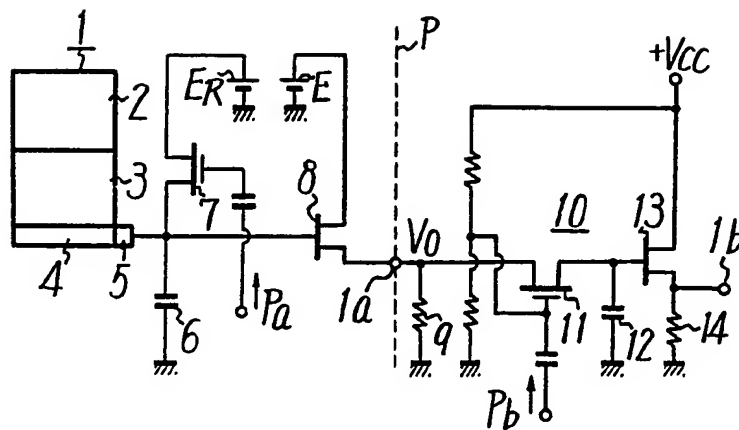
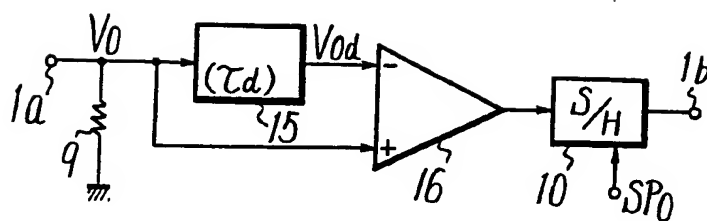
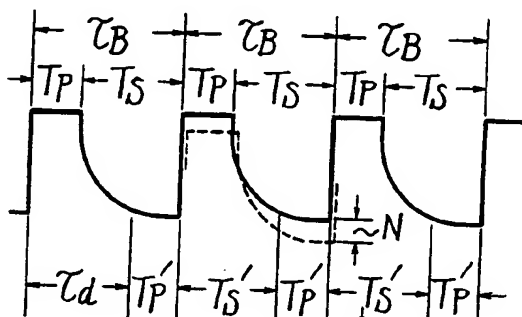
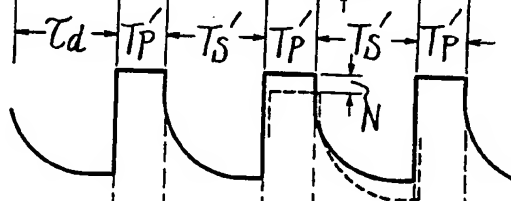
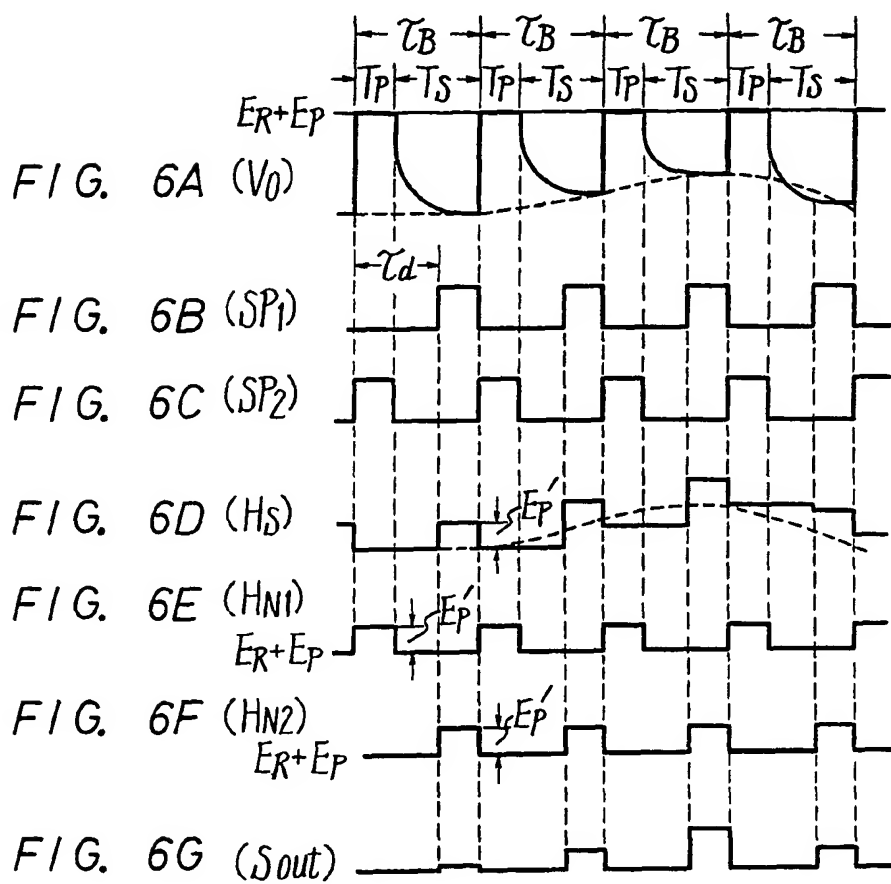
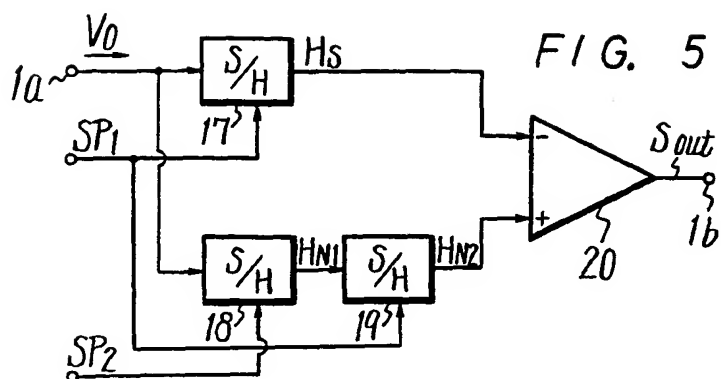


FIG. 3

FIG. 4A (V_0)FIG. 4B (V_{0d})FIG. 4C (SP_0)



SPECIFICATION

Signal pick-up circuit arrangements

5 This invention relates to signal pick-up circuit arrangements.

Figure 1 of the accompanying drawings is a circuit diagram showing an example of a previously proposed output or signal pick-up circuit for a charge coupled device (CCD) image sensor. In this example, the CCD image sensor is of the frame transfer type, and the minority carriers which are stored to represent the information are electrons. In Figure 1, the portion to the left of a dotted line P is the CCD image sensor which is formed on one integrated circuit chip and the portion to the right is a sampling and hold circuit serving as a wave shaping circuit.

The CCD image sensor comprises an image pick-up device 1 with an output terminal 1a, and comprising a photo-sensitive area 2, a storage area 3 for the photo-sensitive area 2, a read-out register 4 for the storage area 3, and an output gate and output diode portion 5 which is reversely biased.

The signal charge produced in the photo-sensitive area 2 is transferred to the storage area 3, and in the photo-sensitive area 2 a photo-electric conversion is carried out such that the signal charge temporarily stored in the storage area 3 is transferred to the read-out register 4 at every one line in the horizontal direction and supplied in time multiplex through the output gate and output diode portion 5. The output terminal of the output gate and output diode portion 5 is grounded through a capacitor 6 and also connected to the source of a field effect transistor (FET) 7 which has the drain supplied with a dc voltage E_R and the gate supplied with a pre-charge pulse P_a (Figure 2A of the accompanying drawings) which is synchronized with the transfer clock signal for the read-out register 4. The connection point between the output gate and diode portion 5 and the capacitor 6 is connected to the gate of an FET 8 which has the drain supplied with a dc voltage E and the source connected to the output terminal 1a.

During a time interval T_p within which the pre-charge pulse P_a is at a high level as shown in Figure 2A, the FET 7 is ON and hence the capacitor 6 is pre-charged up to the voltage E_R . When a time interval T_s within which the pre-charge pulse P_a is at a low level arrives, the FET 7 turns OFF and hence the voltage across the capacitor 6 becomes low in response to the output signal charge. Therefore, when the voltage E_R is taken as a reference level, the voltage across the capacitor 6 in the interval T_s becomes the signal level.

In this case, since the pulse P_a is synchronized with the transfer clock signal for the read-out register 4, a charge detected output voltage V_O , in which the pre-charge level and the signal level will repeat at every one stage portion of the read-out register 4, that is at every bit portion thereof, appears across the capacitor 6 and this voltage V_O is supplied to the output terminal 1a through the FET 8 which forms a buffer amplifier (Figure 2B of the accompanying drawings).

In this example, in practice, the pulse P_a passes

into the signal path through the stray capacitance between the gate and the source of the FET 7, so that a spurious voltage component E_p caused by the pulse P_a is superimposed on the output voltage V_O developed at the output terminal 1a, as shown in Figure 2B. Since the spurious voltage component E_p is approximately constant, no trouble will occur even if a signal higher than the voltage E_R by the amount of the spurious voltage component E_p is taken as the reference level for the signal level. Therefore, no trouble in fact occurs even if the voltage $E_R + E_p$, which is higher than the normal pre-charge level by the spurious voltage component E_p , is taken as the pre-charge level.

The output voltage V_O thus supplied to the output terminal 1a is supplied to a sampling and hold circuit 10 or to the drain of an FET 11 therein for sampling. The FET 11 is supplied at its gate with a sampling pulse P_b which has a high level in the signal level interval T_s of the output voltage V_O as shown in Figure 2C of the accompanying drawings, so that the FET 11 turns ON within the high level interval of the sampling pulse P_b and hence the signal level of the output voltage V_O is sampled. Then, a capacitor 12 for holding in the sampling and hold circuit 10 is charged to the signal level of the sampled signal or discharged, and hence the signal level is held in the capacitor 12. A held voltage V_H across the capacitor 12 is derived through an FET 13 forming a buffer amplifier to an output terminal 1b. Load resistors 9 and 14 are provided for the FETs 8 and 13.

When the charge stored in the CCD image sensor is derived after being converted into a voltage as described above, it is necessary that when the minority carriers are electrons, the capacitor 6 is pre-charged at every one bit. In the pre-charge operation, however, noises such as internal noise in the FET 7 and power source noise for the FET 7 are generated, and the reference pre-charge level is caused to fluctuate due to the noises. Moreover, a level N of the noises produced in the pre-charge interval is held by the capacitor 6 in the one-bit interval τ_a which equals $T_p + T_s$, or the noise is sample-held and appears in the output. As a result, the output voltage V_O fluctuates, as shown by the dotted line in Figure 2B, due to the noise, and hence the signal level in the interval T_s also fluctuates. Accordingly, if the signal level portion of the output voltage V_O is merely sampled and held as in the example of Figure 1, the noise component is mixed into a signal component S and then supplied to the output.

According to the present invention there is provided a signal pick-up circuit arrangement comprising:
an image pick-up device including a charge transfer element and for producing an output charge corresponding to an image;
first means for receiving said output charge from said image pick-up device and for producing a charge detection signal including a reference level portion and a signal portion which is derived by charging or discharging a capacitance in response to said output charge, said reference level portion and said signal portion each being repeated in corres-

pondence with each image element of said pick-up device; and
 second means for deriving a difference output between said reference level portion and said signal portion.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like references designate like elements, and in which:

Figure 1 is a circuit diagram showing a previously proposed charge detecting circuit which is used as an output deriving circuit of a CCD solid state image pick-up device;

Figures 2A to 2C are waveform diagrams used to explain the operation of the example of Figure 1;

Figure 3 is a diagram showing part of an embodiment of signal pick-up circuit arrangement according to the invention.

Figures 4A to 4C are waveform diagrams used to explain the operation of the embodiment of Figure 3;

Figure 5 is a diagram showing part of another embodiment of the invention; and

Figures 6A to 6G are waveform diagrams used to explain the operation of the embodiment of Figure 5.

The embodiments to be described make use of the fact that the noise level is constant in a one-bit interval τ_B and no signal component is present in the pre-charge interval T_p , and they eliminate the noise by obtaining the level difference between the levels in the pre-charge interval T_p and the signal level interval T_S .

An embodiment of signal pick-up circuit arrangement according to the invention will now be described with reference to Figure 3 which shows only part of the embodiment, since the remainder is substantially the same as that of the example of Figure 1, in particular the same as the part to the left of the dotted line P in Figure 1.

The output voltage V_O (Figure 4A) derived at the output terminal 1a is fed to a delay circuit or line 15 and delayed therein by τ_d (0 is less than τ_d is less than τ_B) as a signal V_{Od} (Figure 4B). This delayed signal V_{Od} is supplied to the inverting input terminal of a differential amplifier 16 which is also supplied at its non-inverting input terminal with the undelayed signal V_O . Thus, the differential amplifier 16 produces a difference output between the signal V_O and V_{Od} .

The output from the differential amplifier 16 is fed to the sampling and hold circuit 10 as in the example of Figure 1. In this embodiment, the sampling and hold circuit 10 is supplied with a sampling pulse SP_O (Figure 4C) whose period is τ_B and which becomes the level "1" in a pre-charge interval T_p of the signals V_{Od} , and hence the value of the output from the differential amplifier 16 in the period T_p is sample-held.

During the pre-charge period T_p of the signal V_{Od} , one input signal V_O to the differential amplifier 16 is the signal component plus the noise component and the other input signal V_{Od} thereto is only the noise component, so that the output from the differential amplifier 16 in this period T_p becomes such that the noise component is subtracted or removed from the original output signal V_O . Accordingly, the signal

level, from which the noise is removed, is sample-held in the sampling and hold circuit 10 and then supplied as the output to the output terminal 1b. In Figures 4A and 4B, the dotted lines show the respective detected signals containing noise.

In the embodiment of Figure 3, in order effectively to carry out the operation of subtracting the noise component from the signal component with the noise component in the differential amplifier 16, it is desired that the above operation is carried out at the last portion of the signal level period T_S where the signal level becomes correct. Therefore, for the delay time τ_d of the delay line 15; τ_d is approximately equal to T_S minus the duration length of T_p is the optimum.

Of course, if the pulse width of the sample pulse SP_O is within the period T_p , the pulse width of the pulse SP_O could be shorter than T_p .

Another embodiment of the invention is shown in Figure 5. In this embodiment, in place of the delay circuit 15 used in the embodiment of Figure 3, a sampling and hold circuit is employed to delay the signal V_O .

In detail, the output signal V_O (Figure 6A) developed at the output terminal 1a is fed to a sampling and hold circuit 17 which is also supplied with a sampling pulse SP_1 (Figure 6B) which has the period τ_B , the front edge delayed from that of the pre-charge interval T_p of the output signal V_O by $\tau_d + \tau_B - T_p$, and a pulse width equal to the period T_p . Thus, the signal level portion of the output signal V_O is sample-held in the sampling and hold circuit 17 as a held output H_S as shown in Figure 6D. The held output H_S is fed to the inverting input terminal of a differential amplifier 20.

The output signal V_O is also supplied to a sampling and hold circuit 18 which is also supplied with a sampling pulse SP_2 (Figure 6C) which becomes "1" during the pre-charge interval T_p of the signal V_O . Thus, the level of the signal V_O in the interval T_p is sample-held in the sampling and hold circuit 18. A held output H_{N1} (Figure 6E) therefrom is fed to a further sampling and hold circuit 19 which is also supplied with the sampling pulse SP_1 . Thus, the held output H_{N1} is sample-held in the sampling and hold circuit 19. A held output H_{N2} (Figure 6F) therefrom is supplied to the non-inverting input terminal of the differential amplifier 20.

Pulsating voltages E_p in the respective held outputs H_S , H_{N1} and H_{N2} shown in Figures 6D, 6E and 6F are spurious pulse components which are generated by the fact that the sampling pulses SP_1 and SP_2 respectively pass into the output signal through the capacitance between the gate and source of FET 11 (Figure 1) in the sampling and hold circuit 10.

In this case, since the held output H_S from the sampling and hold circuit 17 is the sampled value of the output V_O in its signal interval T_S , the output H_S includes the signal component and the noise component. While, since the held output H_{N1} from the sampling and hold circuit 18 is the sampled value of the output V_O in its pre-charge interval T_p , the output H_{N1} includes no signal component and only the noise component. Accordingly, the noise component can be removed by subtracting the output H_{N1}

from the output H_S . However, since both outputs H_S and H_{N1} are sample-held outputs of the output V_O at different times, there is a phase difference between the spurious pulses in the respective outputs, as apparent from Figures 6D and 6E. Therefore, if the difference between the outputs H_S and H_{N1} is obtained, the spurious pulses appear as they are.

In the embodiment of Figure 5, however, the output H_{N1} is further sample-held by the sampling pulse SP_1 , so that the spurious pulse appearing in the held output H_{N2} from the sampling and hold circuit 19 is the same in phase as that appearing in the held output H_S . In other words, the sampling and hold circuits 18 and 19 carry out the same operation as that of the delay line 15 in the embodiment of Figure 3. Thus, the differential amplifier 20 supplies an output S_{out} to the output terminal 1b, which includes no noise component and in which the spurious pulse upon the sampling-hold operation is suppressed sufficiently as shown in Figure 6G.

In the above embodiment, the minority carriers stored in the CCD are electrons, so upon detecting the charge, the capacitor 6 is previously charged to the reference level and then discharged in response to the charge. However, when the minority carriers are holes, the stored charge in the capacitor 6 is previously discharged to the reference level and the capacitor 6 is charged in response to the charge.

The invention can be applied not only to CCD charge transfer devices, but also to other charge transfer elements such as bucket bridge devices with the same effect. Moreover, the invention can be applied to a CCD image pick-up device of interline, rather than frame transfer, type.

CLAIMS

1. A signal pick-up circuit arrangement comprising:
an image pick-up device including a charge transfer element and for producing an output charge corresponding to an image;
first means for receiving said output charge from said image pick-up device and for producing a charge detection signal including a reference level portion and a signal portion which is derived by charging or discharging a capacitance in response to said output charge, said reference level portion and said signal portion each being repeated in correspondence with each image element of said image pick-up device; and
second means for deriving a difference output between said reference level portion and said signal portion.

2. An arrangement according to claim 1 wherein said second means derives said difference output between a signal which is produced by delaying said charge detection signal and the undelayed said charge detection signal, and sample-holds a reference level portion of said delayed signal.

3. An arrangement according to claim 2 wherein said second means includes a delay circuit for delaying said charge detection signal and a differential amplifier for deriving said difference output.

4. An arrangement according to claim 1 wherein

said second means derives said difference output from a sample-held output of the signal portion of said charge detection signal and a sample-held portion of the reference level portion of said charge detection signal.

5. An arrangement according to claim 4 wherein said second means includes a sample-hold circuit for sample-holding the signal level portion of said charge detection signal, and two sample-hold circuits for sample-holding a pre-charge level portion of said charge detection signal and delaying the same.

6. A signal pick-up circuit arrangement substantially as hereinbefore described with reference to Figure 3 of the accompanying drawings.

7. A signal pick-up circuit arrangement substantially as hereinbefore described with reference to Figure 5 of the accompanying drawings.

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